CLAIMS

What Is Claimed Is:

1. A process for using a mask having a first composition to aid in forming nanowires having a second composition, comprising:

(a) providing an etchable layer having said second composition and having a buried insulating layer beneath a major surface thereof;

(b) growing self-assembled nanowires having said first composition on said major surface; and

(c) anisotropically etching portions of said etchable layer down to said insulating layer, using said self-assembled nanowires as a mask, to form said nanowires of said second composition.

2. The process of Claim 1 wherein after step (b), a separate molecular or atomic species is deposited on said self-assembled nanowires that preferentially bonds to said self-assembled nanowires so as to enhance a differential etch rate between said nanowires and said etchable layer.

3. The process of Claim 1 wherein said second composition is either a semiconductor material selected from the group consisting of Si, Ge, Ge_xSi_{1-x} where $0 < x < 1$, GaAs, InAs, AlGaAs, InGaAs, AlGaAs, GaN, InN, AlN, AlGaN, and InGaN or a metal selected from the group consisting of Al, Cu, Ti, Cr, Fe, Co, Ni, Zn, Ga, Nb, Mo, Pd, Ag, In, Ta, W, Re, Os, Ir, Pt, and Au, and alloys thereof.

4. The process of Claim 3 wherein said second composition comprises silicon.

5. The process of Claim 1 wherein said buried insulating layer comprises an oxide or a nitride or a mixture thereof or a metal fluoride.

6. The process of Claim 5 wherein said oxide comprises silicon dioxide or wherein said nitride comprises silicon nitride or wherein said mixture comprises silicon oxynitride or wherein said metal fluoride comprises calcium fluoride.

7. The process of Claim 1 wherein said etchable layer has a thickness within a range of about 1 to 100 nm.

8. The process of Claim 1 wherein said self-assembled nanowires are epitaxially grown on said etchable layer, whereby an interfacial plane is formed between said self-assembled nanowires and said etchable layer, wherein said material comprising said self-assembled nanowires is closely-lattice matched to said material comprising said etchable along one major crystallographic axis on said interfacial plane, but has significant lattice mismatch along all other major crystallographic axes on said interfacial plane, said method comprising:

(a) selecting as said material a composition that is closely-lattice matched to said etchable material along one major crystallographic axis, but has significant lattice mismatch along all other crystallographic axes in said interfacial plane;

(b) cleaning a surface of said substrate so that said surface has an atomically flat, regular atomic structure on terraces and has regular steps and so that impurities are removed; and

(c) epitaxially growing said self-assembled nanowires on said etchable layer.

9. The process of Claim 8 wherein said self-assembled nanowires have a width within a range of about 1 to 100 nm, a height within a range of about 0.2 to 100 nm, and a length within a range of about 10 nm to 10 μm.

10. The process of Claim 8 wherein said self-assembled nanowires comprise a metal silicide and wherein said etchable layer comprises silicon, in which said metal is deposited on said silicon layer and said metal is converted to said metal silicide.

11. The process of Claim 10 wherein said metal silicide is represented by the formula MSi_2, where M is selected from the group consisting of scandium, yttrium, and rare earths.

12. The process of Claim 11 wherein said rare earths are selected from the group consisting of erbium, dysprosium, gadolinium, thulium, holmium, terbium, and samarium.

13. The process of Claim 8 wherein said forming in step (c) is performed with an in situ electron-beam evaporator, employing layer temperatures ranging from room temperature to 800°C.

14. The process of Claim 13 wherein after said forming in step (c), said nanowires formed on said silicon layer are annealed to complete any chemical reaction between said nanowires and said etchable layer.

15. The process of Claim 14 wherein said annealing is performed at a temperature within a range of 575° to 800°C for a time of up to 5 minutes.

16. The process of Claim 1 wherein reactive ion etching is used to anisotropically etch said etchable layer relative to said self-assembled nanowires.

17. The process of Claim 16 wherein said etchable layer has an etching rate in said anisotropic etching that is at least twice that of said self-assembled nanowires.

18. The process of Claim 1 wherein after step (c), said self-assembled nanowires are removed from said formed nanowires.

19. The process of Claim 18 wherein said self-assembled nanowires are removed from said formed nanowires by selective chemical etching.

20. The process of Claim 19 wherein said self-assembled nanowires have an etching rate during said selective chemical etching that is at least twice that of said etchable layer.